REMARKS

By the present amendment and response, independent claim 1 has been amended to overcome the Examiner's objections and claim 2 has been canceled. Thus, claims 1 and 3-11 remain in the present application. Reconsideration and allowance of outstanding claims 1 and 3-11 in view of the above amendments and the following remarks are requested.

A. Confirmation of Applicant's Election

Applicant hereby confirms election of claims 1-11 (now claims 1 and 3-11), without traverse, for prosecution in the present application.

B. Drawing and Specification Amendments

Applicant has amended the drawings as requested by the Examiner and the amended drawings are attached hereto. Moreover, the specification has been amended to correspond to the amended drawings. No new matter has been introduced. Clean and marked up versions of the amended specification are included herewith.

C. Objection to the Abstract

Applicant submits that its comments below with respect to the term "pinned transferred gate" overcome the Examiner's objection to the Abstract.

D. Claim Rejections

1. Claim rejection under 35 USC §112, first paragraph

The Examiner has rejected claims 1-11 under 35 USC §112, first paragraph. Applicant has amended independent claim 1 to overcome the Examiner's 35 USC §112,

first paragraph, rejection. Applicant's remarks below further illustrate that the amended claims overcome the Examiner's 35 USC §112, first paragraph, rejection.

2. Claim rejections under 35 USC §102 and 35 USC §103

The Examiner has rejected claims 1 and 5-8 under 35 USC §102(e) as being anticipated by Guidash (Pub. No. US 2002/0121656 A1) (hereinafter, "Guidash"). The Examiner has separately rejected claims 1, 2, and 5 under 35 USC §102(e) as being anticipated by Figure 1 of Zheng, et al. (Pub. No. US 2002/0121655 A1) (hereinafter, "Zheng"). The Examiner has also rejected claims 1, 3-4, and 6 under 35 USC §102(e) as being anticipated by Figure 5 of Zheng. For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claim 1, is patentably distinguishable over either Guidash or Zheng. However, Applicant reserves the right to provide declarations and/or documents under 37 CFR §1.131 to "swear behind" the respective effective filing dates of Guidash and/or Zheng.

Subject to Applicant's reserved right to establish priority of the present invention under 37 CFR §1.131, Applicant submits that the present invention, as defined by amended independent claim 1, teaches, among other things, "a pinned transfer gate formed by an implanted P type region within an implanted N type transfer region, the implanted P type region being pinned to a potential of a P type substrate, wherein the P type substrate surrounds the N type transfer region, and wherein the transfer gate is disposed to transfer charge between the photoreceptor and the sense node."

Initially, it is noted that a patent applicant is allowed to be his or her own "lexicographer." As such, Applicant has utilized the phrase "pinned transfer gate" to define a certain device configuration as discussed below. In other words, the phrase "pinned transfer gate" is not required to be known in the art, or used in the art at all, or used in the art in exactly the same manner as defined by a patent applicant. Having the above in mind, Applicant respectfully draws the Examiner's attention to the following exemplary parts of the present application which define and use the phrase "pinned transfer gate" as recited by amended independent claim 1.

The present application states: "The pinned transfer gate 206 is formed from a shallow p++ implanted pinned region 219 in an n-implanted transfer region 221 in the p-type substrate 202." Page 6, lines 18-19. The present application further states: "The pinned transfer gate is "pinned" because the p++ doped pinned region 219 is tied (or "pinned") to the potential of the substrate 202, typically ground or zero volts." Page 7, lines 5-7.

Moreover, the present application notes that: "the pinned transfer region omits a transistor gate structure (e.g., such as the photoreceptor readout gate 216 provided for the photoreceptor 204). Instead, the pinning sets up a potential well profile that allows charge to transfer through the pinned transfer gate 206 depending on the photoreceptor readout clocks 116 as will be discussed in more detail below." Page 6 line 23 through page 7, line 4. This is explained further in the application, which states: "Note that the readout potential well 228 is shallower than the transfer potential well 230, established by

the pinned transfer gate 206. As a result, electrons captured by the integration potential well 226 propagate through the transfer potential well 230 and into the sense node potential well 232." Page 8, lines 11-15.

Thus, as claimed in amended independent claim 1, the "pinned transfer gate" is formed by an implanted P type region within an implanted N type transfer region, the implanted P type region being "pinned" to a potential of a P type substrate, wherein the P type substrate surrounds the N type transfer region, and wherein the transfer gate is disposed to transfer charge between the photoreceptor and the sense node. It is noted that the "pinning" is accomplished because the implanted P type region is of the same conductivity type as the P type substrate. Thus, the electrical "pinning" of the implanted P type region to the ground potential is automatically accomplished by virtue of the fact that the P type substrate is at ground potential.

In sum, the "pinned transfer gate" is a novel configuration within the context of a CMOS imaging device and when used for the purpose of transferring charges not through the action of a transistor gate - which is used in the references cited by the Examiner - but through the action of setting up different potential wells, as explained in the present application. Amended independent claim 1 defines such structure which is used to set up different potential wells for integrating charges and then transferring the integrated charges to be read at a sense node - and more specifically at the implanted N+ contact region 223 - by, for example, the source follower output amplifier 212 in Figure 2B.

As such, the physical structure and operation of the "pinned transfer gate" of the present application is in marked contrast with the "transfer gates" utilized in the cited references. In Guidash, transfer transistor 14 is a typical transistor having a source and drain. For example, Guidash states that "transfer transistor 14 must have its gate and drain silicided 34 in order to retain desired transistor performance." Paragraph 30 of Guidash. Manifestly, transfer transistor 14 is not formed "by an implanted P type region within an implanted N type transfer region, the implanted P type region being pinned to a potential of a P type substrate, wherein the P type substrate surrounds the N type transfer region" as required by amended claim 1.

With respect to Zheng, both the p-MOSFET of Figure 1 and transfer gate 83 of Figure 5 are typical transistors having respective gates and source and drain regions. Manifestly, neither the p-MOSFET of Figure 1 nor transfer gate 83 of Figure 5 is formed "by an implanted P type region within an implanted N type transfer region, the implanted P type region being pinned to a potential of a P type substrate, wherein the P type substrate surrounds the N type transfer region" as required by amended claim 1.

The Examiner has also rejected claims 9-11 under 35 USC §103(a) as being unpatentable over Zheng in view of Turko, et al. (U.S. Patent 5,121,214) (hereinafter, Turko). As discussed above, amended independent claim 1 is patentable over Zheng and, as such, dependent claims 9-11 are, *a fortiori,* patentable over Zheng, or its combination with Turko, for added limitations therein.

E. Conclusion

Based on the foregoing reasons, the present invention, as defined by amended independent claim 1 and claims 3-11 depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, an early allowance of outstanding claims 1 and 3-11 is respectfully requested.

Please note that Applicant's attorneys have changed. Applicant has filed a "revocation and power of attorney" to formally effect this change. The contact information of Applicant's new attorneys appear below.

Respectfully Submitted,
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Signature Date

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

The paragraph beginning at line 6 of page 5 has been amended as follows:

Figure 1A shows [a pinned transfer gate (PTG) pixel with] a diagram of an imager cell control and readout [circuitry] circuit.

The paragraph beginning at line 8 of page 5 has been amended as follows:

Figure 2A shows a [PTG pixel with a poly photoreceptor] diagram of a photoreceptor readout clock.

The paragraph beginning at line 9 of page 5 has been amended as follows:

Figure 3A shows a [PTG pixel cell with a "poly hole" photoreceptor] diagram of a photoreceptor readout clock.

The paragraph beginning at line 10 of page 5 has been amended as follows:

Figure 4A shows a [PTG pixel cell with a "thin gate" photoreceptor] diagram of a photoreceptor readout clock.

The paragraph beginning at line 19 of page 5 has been amended as follows:

With regard first to Figure 1B, an imager cell 100 (descried in more detail below) includes a photoreceptor 102, a transfer gate 104, and a sense node 106. A reset transistor 108 is provided to reset the sense node 106, and an output amplifier 110 provides sense node buffering when the sense node 106 is readout to the column bus through the select transistor 112. [Also illustrated in] Figure 1A [is] shows control circuitry 114, which [that] produces photoreceptor readout clocks 116, sense node reset clocks 118, and imager cell readout clocks 120. The control circuitry 114 may generally be implemented as a conventional CMOS imager controller, except with regard to the operating modes described in more detail below and with regard to the applicable integration voltages that setup preselected charge capacity levels in the photoreceptor 102.

The paragraph beginning at line 7 of page 6 has been amended as follows:

Turning next to Figure 2B, that figure presents a more detailed view of an imager cell 200. The imager cell 200 is formed in a p-type substrate 202 and includes a photoreceptor 204, pinned transfer gate 206 and sense node 208. A reset transistor 210 provides a mechanism for resetting the sense node 208 to an initial level, while the source follower output amplifier 212 provides sense node 208 output buffering and amplification. As shown in Figure 2C, [A] a potential well diagram 214 illustrates the variation in electric potential across the imager cell 200.

The paragraph beginning at line 14 of page 6 has been amended as follows:

As shown in Figure 2B, the photoreceptor 204 is formed as a "poly photogate" including a photoreceptor readout gate 216, supporting photoreceptor gate oxide 218, and the p-type substrate 202. Other implementations of photoreceptors are also suitable however, including photodiodes.

The paragraph beginning at line 10 of page 7 has been amended as follows:

The operation of the photoreceptor 200 in Figure 2B is discussed with reference to the potential well diagram 214 in Figure 2C and the photoreceptor readout clock 220 in Figure 2A. Note that the photoreceptor readout clock 220 varies between a V+ level during an integration period 222 and a V- level during a readout period 224. The duration of the integration period 222 and the readout period 224 vary in accordance with the desired operating speed of the photoreceptor 200. In one implementation, for example, the duration of the integration period 222 may be approximately 1 second, while the duration of the readout period 224 may be approximately $1/30^{th}$ of a second.

The paragraph beginning at line 15 of page 9 has been amended as follows:

Turning next to Figure 3B, that figure shows an implementation of an imager cell 300 employing a poly-hole gate 302 and an optional p++ pinned aperture region 304 (with a corresponding integration potential well 306, which is shown in Figure 3C, in the

substrate 202 in Figure 3B). The operation of the imager cell 300 with regard to the photoreceptor readout clock 220 shown in Figure 3A is substantially similar to that described above in Figure 2A with regard to the imager cell 200 in Figure 2B. Note, however, that the imager cell 300 provides enhanced response to blue light because the photoreceptor readout gate 216 has had material removed to form the photoreceptor readout gate light aperture 308 above the photoreceptor 204. As a result, many photons impinge up the photoreceptor 204 without passing through polysilicon gate material. Because blue photons tend to be absorbed when passing through polysilicon gate material, the light aperture 308 allows more blue photons to reach the photoreceptor 204. The imager cell 300 has correspondingly increased response to blue light. Note also that a micro-lens (not illustrated) focused on the "poly hole" region may be provided above the light aperture 308 to help focus photons into the photoreceptor 204.

The paragraph beginning at line 15 of page 10 has been amended as follows:

Figure 4B presents an additional implementation of an imager cell 400. The imager cell 400 includes a thin photoreceptor readout gate 402. The imager cell 400, like the imager cell 300, provides increased sensitivity to blue light. Generally, a photoreceptor readout gate more than 2000 Angstroms thick absorbs significant amounts of blue light. Thus, the thin photoreceptor readout gate 402 is fabricated generally 2000 Angstroms or less in thickness, for example between 50 and 2000 Angstroms. However, the thickness of the thin photoreceptor readout gate 402 may also be varied in accordance

with the charge capacity desired in the photoreceptor (which depends on the voltage applied to the photoreceptor readout gate during integration). For example, for 3.3 volt operation a gate thickness of 50-65 Angstroms may be used, while for 5.0 volt operation a gate thickness of 100-110 Angstroms may be used.

The paragraph beginning at line 4 of page 11 has been amended as follows:

The operation of the imager cell 400 with regard to the photoreceptor readout clock 220 in Figure 4A is similar to that described above in Figure 2A with regard to the imager cell 200 in Figure 2B. Also, the variation in electric potential across the imager cell 400 shown in Figure 4C is similar to that described above in Figure 2C with regard to the imager cell 200 in Figure 2B.

The paragraph beginning at line 15 of page 11 has been amended as follows:

In addition, the method 500 fabricates (508) a photoreceptor readout gate, e.g., 216, above the photoreceptor 204. As discussed above with regard to Figure 4B, the photoreceptor readout gate may be fabricated with a thickness of less than 2000 Angstroms, for example, 400 Angstroms. The method 500 also fabricates (510) a reset transistor 108 and an output amplifier 110 for the sense node 208. Note that the pinned transfer gate 206 is generally fabricated (512) as a p-doped pinned region in an n-doped transfer region. As discussed above with regard to Figure 3B, the method 500 may fabricate (512) a light aperture 308 above the photoreceptor 204, as well as fabricate

(514) a pinned aperture region 304 in the photoreceptor 204 and an anti-reflective coating above the photoreceptor 204.

In the Claims:

Claim 1 has been amended as follows:

1. (Once Amended) An imager cell comprising:

a photoreceptor;

a sense node; and

a pinned transfer gate formed by an implanted P type region within an implanted N type transfer region, the implanted P type region being pinned to a potential of a P type substrate, wherein the P type substrate surrounds the N type transfer region, and wherein the transfer gate is disposed to transfer charge between the photoreceptor and the sense node.

Claim 2 has been canceled.